REMARKS

Claims 1-10 are pending. Claims 1, 3, and 5 have been amended. No new matter has been added by way of this amendment. Reconsideration of the application is respectfully requested.

Claims 1 and 3-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,366,292 to *Allen* in view of U.S. Patent No. 6,229,513 to *Nakano* et al., while claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the same references, and in further view of U.S. Patent No. 6,404,533 to *Fergusson*. This rejection is respectfully traversed.

U.S. Patent No. 6,366,292 to *Allen* relates to a method apparatus for scaling an enhancing a digital image for a wide variety of applications, such as adapting digital image data for various video formats (see col. 1, line 35-40).

Set forth on page 2, paragraph 3 of the Office Action is the statement that:

> "Allen teaches LCD monitor (38) comprising: a panel module having a gate driver and a source driver; a control board disposed on a first side of the panel module, comprising: an input interface (32) (Figs. 3 and 4) for receiving plural types video signal, adapted to select a first type video signal; a scaler module (34) (Figs. 3 and 4) comprises a time control unit (54, 56, 58) (Fig. 4), and is provided to receive the first digital video signal; a micro-processing device (42) (Fig. 3), adapted to output a control signal that controls the scaler module (34) to generate a gate/source-driving signal for the gate driver and the source driver according to the first digital video signal (col. 3, lines 53-67, col. 4, lines 1-19, lines 56-67, and col. 5. lines 1-2).
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> Allen differs from claim 1 in that he does not specifically teach a cover structure conjugating the frame structure in the aspect of the first side, and covering upon the first side of the panel module and the control board thereon. However, referring to Figs. 10-12, Nakano teaches a frame structure (SHD), covering the periphery of the panel module; and a cover structure (LF1, LF2) conjugating the frame structure (SHD) in the aspect of the first side, and covering upon the first side of the panel module and the control board thereon (col. 14, lines 28-55 and col. 15, lines 14). Therefore, it would have been obvious ton one of ordinary skill in the art at the time the invention was made

to incorporate the frame structure and cover structure as taught by Nakano in the system of Allen in order to protect the inner electronic devices."

With respect to claim 1, Applicants respectfully wish to point out that the foregoing rejection fails to provide an element-by-element analysis of this claim. For example, although it is true that the *Allen* patent discloses that "a processor 42 coordinates the operations of the video scaler module 34 and OSD module 40"(see col. 4, lines 1-2), this reference fails to teach or suggest the limitation "a micro-processing device, adapted to output a first control signal that controls the scaler module to generate a gate/source-driving signal for the gate driver and the source driver according to the first digital video signal..." as set forth in claim 1 of the present application. Accordingly, Applicants respectfully assert that the processor 42 set forth in *Allen* is not equivalent in structure or function to the micro-processor set forth in claim 1 of the present invention.

U.S. Patent No. 6,229,513 to *Nakano* et al. relates to techniques for use in a liquid crystal display apparatus for lowering the frequency of clock signals that are sent to driving devices. According to this patent, this is accomplished by using driving devices that are similar to those encountered in conventional liquid crystal display apparatuses, without increasing the bus width of a bus line for transmitting the display data therethrough (see col. 2, lines 61-67). However, this patent fails to teach the limitation "a micro-processing device, adapted to output a first control signal that controls the scaler module to generate a gate/source-driving signal for the gate driver and the source driver according to the first digital video signal..." and hence, *Nakano* et al. fail to cure the deficiency of the *Allen* patent.

In so far as the combination of the *Allen* and *Nakano* et al. fails to specifically teach the micro-processing device disclosed in the present application, it is apparent that it is the Examiner's

belief that it would have been obvious to obtain the "micro-processing device, adapted to output a first control signal that controls the scaler module to generate a gate/source-driving signal for the gate driver and the source driver according to the first digital video signal" as set forth in claim 1. However, without some teaching or suggest in the prior art, such a conclusion is unwarranted.

Moreover, claim 1 recites a control board comprising an input interface, a scaler module and a micro-processing device. However, neither the *Allen* nor the *Nakano* et al. patents, neither individually nor in combination, disclose a control board that integrates an input interface, a scaler module and a micro-processing device therein. That is, there is only one PCB (i.e., the control board 20) in one LCD monitor of the present claimed invention so as to simplify the manufacturing process. As a result, the costs associated with training laborers and fabricating the claimed device is greatly reduced, and the production yield is further improved.

Accordingly, Applicants respectfully assert that the Office Action fails to provide a definite indication in the combined references of each corresponding element that is set forth and claimed in the present application. It is therefore Applicants' belief that the combination of *Allen* and *Nakano* et al. does not teach, nor does it suggest that it would it have been obvious to one of ordinary skill in the art to use, a control board that integrates the input interface, the scaler module and the micro-processing device into one component, as set forth in claim 1. Based on the differences between claim 1 and the combination of the *Allen* and *Nakano* et al. patents mentioned above, the Office Action has failed to establish a *prima facie* case of obviousness with respect to claim 1. Therefore, it is Applicants' belief that claim 1 is allowable over the cited references.

U.S. Patent No. 6,404,533 to *Fergusson* relates to an optical amplitude modulator for modulating signals for transmission by a fibre optic link (see col. 2, lines 30-33). However,

Fergusson only discloses a video signal comprising an EDID signal but does not disclose all the elements and features as set forth in claim 1 and hence, fails to cure the deficiency of the *Allen* and *Nakano* et al. combination. Claim 2 depends from claim 1, it is therefore Applicants' belief that claim 2 is also allowable over the cited references.

Insofar as claims 3-10 depend from claim 1, it is Applicants' belief that these claims are also allowable.

Based on the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this Response, or the application in general, a telephone call to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

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